CLAIMS

Please amend the claims as follows:

1. (currently amended) A method of specifying a trace array for a simulation model of an electronic design in a data processing system, said method comprising:

permitting a user to specify one or more design entities within a simulation model with one or more statements in one or more hardware description language (HDL) files, wherein specifying the one or more design entities includes specifying a plurality of signals, functional logic, and any storage elements that define functional operation of the electronic design;

permitting a user to specify, in one or more statements in the one or more HDL files, an instrumentation entity that monitors at least one design entity among the one or more design entities but does not contribute to functional operation of the electronic design, wherein specifying the instrumentation entity includes specifying a trace array within the instrumentation entity and indicating a monitored signal set including at least one signal among the plurality of signals, wherein the trace array concurrently stores multiple values for the monitored signal set obtained over multiple cycles of functional operation of the simulation model, wherein specifying a trace array includes specifying an association between an enumerated value and a value of the at least one signal comprising said monitored signal set; and

storing said one or more HDL files.

2.-5. (canceled)

6. (currently amended) A method of preparing a simulation model of an electronic design within a data processing system, said method comprising:

receiving one or more hardware description language (HDL) files declaring a plurality of design entities forming the electronic design, wherein the plurality of design entities includes a plurality of signals, functional logic, and any storage elements that define functional operation of the electronic design, wherein said one or more HDL files further include one or more statements specifying an instrumentation entity that monitors at least one design entity among the one or more design entities but does not contribute to functional operation of the electronic design,

specifying a trace array within the instrumentation entity, and indicating a monitored signal set including at least one signal among the plurality of signals; and

in response to receipt of the one or more HDL files, parsing and processing said one or more HDL files to generate a simulation model formed of representations of instances of the plurality of the design entities and a trace array within at least one of the instances of the plurality of design entities, wherein the trace array is configured to concurrently store multiple values for the monitored signal set obtained over multiple cycles of functional operation of the simulation model

wherein said parsing and processing said one or more HDL files includes:

creating, within the trace array, storage for multiple values of the monitored signal set;

creating an association between an enumerated value and a value of the at least one signal comprising said monitored signal set; and

placing the simulation model in data storage.

7.-11. (canceled)

12. (currently amended) A method of reporting simulation data obtained by the simulation of an electronic design within a data processing system, said method comprising:

a simulator running a testcase against a simulation model of the electronic design, wherein:

the simulation model is formed of representations of instances of a plurality of design entities,

the instances of the design entities contain a plurality of signals, functional logic, and any storage elements that define functional operation of the electronic design,

each instance of at least a particular design entity of the plurality of design entities contains an instance of an instrumentation entity that monitors the containing instance of the particular design entity but does not contribute to functional operation of the electronic design, and

each instance of the instrumentation entity contains a trace array logically coupled to receive a monitored signal set including at least one signal among the plurality of

signals, wherein the trace array is further logically coupled to receive a control signal among the plurality of signals;

recording trace data for the monitored signal set within the trace array during the running of the testcase, wherein the recording includes concurrently storing within the trace array multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model, wherein recording trace data includes recording, within the trace array, values assumed by the monitored signal set during only those cycles of functional operation during which the control signal is asserted; and

exporting said trace data from said trace array in a trace file and storing said trace file in data storage, wherein exporting the trace data in a trace file includes exporting the trace data in a trace file indicating an association between an enumerated value and a value of said monitored signal set.

13.-15. (canceled)

16. (currently amended) A data processing system, comprising:

means for specifying one or more design entities within a simulation model of an electronic design with one or more statements in one or more hardware description language (HDL) files, wherein the means for specifying the one or more design entities includes means for specifying a plurality of signals, functional logic, and any storage elements that define functional operation of the electronic design;

means for specifying, in one or more statements in the one or more HDL files, an instrumentation entity that monitors at least one design entity among the one or more design entities but does not contribute to functional operation of the electronic design, wherein the means for specifying the instrumentation entity includes means for specifying a trace array within the instrumentation entity and indicating a monitored signal set including at least one signal among the plurality of signals, wherein the trace array concurrently stores multiple values for the monitored signal set obtained over multiple cycles of functional operation of the simulation model, wherein said means for specifying a trace array comprises means for specifying an association between an enumerated value and a value of the at least one signal comprising said monitored signal set; and

means for storing said one or more HDL files.

17.-20. (canceled)

21. (currently amended) A data processing system for preparing a simulation model of an electronic design, said data processing system comprising:

means for receiving one or more hardware description language HDL files declaring a plurality of design entities forming the digital design, wherein the plurality of design entities includes a plurality of signals, functional logic, and any storage elements that define functional operation of the electronic design, wherein said one or more HDL files further include one or more statements specifying an instrumentation entity that monitors at least one design entity among the one or more design entities but does not contribute to functional operation of the electronic design, specifying a trace array within the instrumentation entity, and indicating a monitored signal set including at least one signal among the plurality of signals; and

means, responsive to receipt of the one or more HDL files, for parsing and processing said one or more HDL files to generate a simulation model formed of representations of instances of the plurality of the design entities and a trace array within at least one of the instances of the plurality of design entities, wherein the trace array concurrently stores multiple values for the monitored signal set obtained over multiple cycles of functional operation of the simulation model, wherein said means for parsing and processing said one or more HDL files includes means for creating an association between an enumerated value and a value of the at least one signal comprising said monitored signal set.

22.-26. (canceled)

27. (currently amended) A data processing system, comprising:

means for running a testcase against a simulation model of an electronic design, wherein:

the simulation model is formed of representations of instances of a plurality of design entities,

the instances of the design entities contain a plurality of signals, functional logic, and any storage elements that define functional operation of the electronic design,

each instance of at least a particular design entity of the plurality of design entities contains an instance of an instrumentation entity that monitors the containing instance of the particular design entity but does not contribute to functional operation of the electronic design, and

each instance of the instrumentation entity contains a trace array logically coupled to receive a monitored signal set including at least one signal among the plurality of signals;

means for recording trace data for the monitored signal set within the trace array during the running of the testcase, wherein the recording includes concurrently storing within the trace array multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model; and

means for exporting said trace data from said trace array in a trace file and storing said trace file in data storage, wherein said means for exporting the trace data in a trace file includes means for exporting the trace data in a trace file indicating an association between an enumerated value and a value of said monitored signal set.

28.-30. (canceled)

31. (currently amended) An apparatus comprising a tangible computer usable medium containing program code, said program code including:

means for specifying one or more design entities within a simulation model of an electronic design with one or more statements in one or more hardware description language (HDL) files, wherein the means for specifying the one or more design entities includes means for specifying a plurality of signals, functional logic, and any storage elements that define functional operation of the electronic design;

means for specifying, in one or more statements in the one or more HDL files, an instrumentation entity that monitors at least one design entity among the one or more design entities but does not contribute to functional operation of the electronic design, wherein the means for specifying the instrumentation entity includes means for specifying a trace array within the instrumentation entity and for indicating a monitored signal set including at least one signal among the plurality of signals, wherein the trace array concurrently stores multiple values

for the monitored signal set obtained over multiple cycles of functional operation of the simulation model, wherein said means for specifying a trace array comprises means for specifying an association between an enumerated value and a value of the at least one signal comprising said monitored signal set; and

means for storing said one or more HDL files.

32.-35. (canceled)

36. (currently amended) An apparatus for preparing a simulation model of an electronic design, said apparatus comprising a tangible computer usable medium containing program code, said program code including:

means for receiving one or more hardware description language (HDL) files declaring a plurality of design entities forming the electronic design, wherein the plurality of design entities includes a plurality of signals, functional logic, and any storage elements that define functional operation of the electronic design, wherein said one or more HDL files further include one or more statements specifying an instrumentation entity that monitors at least one design entity among the one or more design entities but does not contribute to functional operation of the electronic design, specifying a trace array within the instrumentation entity, and indicating a monitored signal set including at least one signal among the plurality of signals; and

means, responsive to receipt of the one or more HDL files, for parsing and processing said one or more HDL files to generate a simulation model formed of representations of instances of the plurality of the design entities and a trace array within at least one of the instances of the plurality of design entities, wherein the trace array concurrently stores multiple values for the monitored signal set obtained over multiple cycles of functional operation of the simulation model, wherein said means for parsing and processing said one or more HDL files includes means for creating an association between an enumerated value and a value of said monitored signal set.

37.-41. (canceled)

42. (currently amended) An apparatus comprising a computer usable medium containing program code, said program code including:

means for running a testcase against a simulation model of an electronic design, wherein:

the simulation model is formed of representations of instances of a plurality of design entities,

the instances of the design entities contain a plurality of signals, functional logic, and any storage elements that define functional operation of the electronic design,

each instance of at least a particular design entity of the plurality of design entities contains an instance of an instrumentation entity that monitors the containing instance of the particular design entity but does not contribute to functional operation of the electronic design, and

each instance of the instrumentation entity contains a trace array logically coupled to receive a monitored signal set including at least one signal among the plurality of signals; and

means for recording trace data for the monitored signal set within the trace array during the running of the testcase, wherein the recording includes concurrently storing within the trace array multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model; and

means for exporting said trace data from said trace array in a trace file and storing said trace file in data storage, wherein said means for exporting the trace data in a trace file includes means for exporting the trace data in a trace file indicating an association between an enumerated value and a value of said monitored signal set.

43.-45. (canceled)